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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/910,447	07/19/2001	Toshihiko Higuchi	81754.0064	2754

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EXAMINER
LE, THAO X

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 06/05/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/910,447	Applicant(s) HIGUCHI, TOSHIHIKO	
	Examiner Thao X Le	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 May 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *13-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *7* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 1-12 in Paper No. 9 is acknowledged.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claim 1, 5-6, 8-9, 11-12 are rejected under 35 U.S.C. 102(e) as being anticipated by US Pub 2001/0045608 to Tseng et al.

Regarding to claim 1, Tseng discloses a semiconductor device in fig. 8 comprising: a semiconductor substrate 10, column 6 line 23, a gate electrode ~~40~~ 24, paragraph [0023], formed on the semiconductor substrate through a gate dielectric layer

22, paragraph [0027], first and second impurity diffusion layers 16/18a, paragraph [0029] formed in the semiconductor substrate and opposed to each other with the gate electrode being interposed between them, and a sidewall dielectric layer 20, paragraph [0026], formed on the side surface section of the gate electrode, wherein the gate electrode has a width that gradually increases from a bottom thereof toward an upper surface thereof, and wherein surfaces of the first and second impurity diffusion layers are located at a position higher than an interface between the semiconductor substrate and the gate dielectric layer, fig. 8.

Regarding to claim 5, 6, Tseng discloses a semiconductor device wherein trench isolation region 12 is formed in the semiconductor substrate, and dielectric layer embedded therein, paragraph [0023]

Regarding to claim 8, Tseng discloses a semiconductor device wherein a third impurity diffusion region layer 18b is formed in a portion immediately below the gate electrode in the semiconductor substrate, fig. 8 paragraph [0025].

Regarding to claim 9, Tseng discloses a semiconductor device wherein a metal silicide layer 26 is formed on the first and second impurity diffusion layers, and the gate electrode includes a metal silicide layer 26 on an upper surface thereof, paragraph [0029].

Regarding to claim 11, Tseng discloses a semiconductor device wherein the surfaces of the first and second impurity layers 16 are formed at a position higher than a surface of the element isolation region 12, fig. 8.

Regarding to claim 12, Tseng discloses a semiconductor device wherein the sidewall dielectric layer has an outer surface that is generally vertical with respect to the

surface of the semiconductor substrate, and film thickness that gradually reduces from a bottom thereof toward an upper surface thereof, fig. 8.

5. Claims 1-3, 5-7, 9, 11-12 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent 6,130,454 to Gardner et al.

Regarding to claim 1, Gardner discloses a semiconductor device in fig. 12 comprising: a semiconductor substrate 10, column 6 line 23, a gate electrode 40, column 7 line 43, formed on the semiconductor substrate through a gate dielectric layer 36, column 7 line 39, first and second impurity diffusion layers 52, column 8 line 50, formed in the semiconductor substrate and opposed to each other with the gate electrode being interposed between them, and a sidewall dielectric layer 52, column 9 line 1, formed on the side surface section of the gate electrode, wherein the gate electrode has a width that gradually increases from a bottom thereof toward an upper surface thereof, and wherein surfaces of the first and second impurity diffusion layers are located at a position higher than an interface between the semiconductor substrate and the gate dielectric layer, fig. 12.

Regarding to claim 2, Gardner discloses a semiconductor device wherein a distance between the surface of the first and second impurity diffusion layers and the interface between the semiconductor substrate and the gate dielectric layer is between 0.05 and 0.15 μm, column 7 line 3.

Regarding to claim 3, Gardner discloses a semiconductor device wherein the groove section 20, column 6 line 56, is formed at a specified location in the

semiconductor substrate, and the gate electrode is formed on a bottom surface of the groove section through the gate dielectric layer, fig 1-5.

Regarding to claim 5, 6, Gardner discloses a semiconductor device wherein trench isolation region 12, column 6 line 26, is formed in the semiconductor substrate, and dielectric layer embedded therein, column 6 line 30.

Regarding to claim 7, Gardner discloses a semiconductor device wherein the first and second impurity diffusion layer includes an extension region 48, column 8 line 55.

Regarding to claim 9, Gardner discloses a semiconductor device wherein a metal silicide layer 54 is formed on the first and second impurity diffusion layers, and the gate electrode includes a metal silicide layer 54 on an upper surface thereof, column 8 lines 60-64.

Regarding to claim 11, Gardner discloses a semiconductor device wherein the sidewall dielectric 52 is formed on the bottom surface of the first and second impurity diffusion layers are formed at a position higher than a surface of the element isolation region.

Regarding to claim 12, Gardner discloses a semiconductor device wherein the sidewall dielectric layer has an outer surface that is generally vertical with respect to the surface of the semiconductor substrate, and film thickness that gradually reduces from a bottom thereof toward an upper surface thereof, fig. 12.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 4, 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent 6,130,454 to Gardner et al, and further in view of US Patent 6,201,278 to Gardner et al.

Regarding to claim 4, Gardner discloses a semiconductor device wherein the gate electrode 40 may be formed by depositing the conductive material or semiconductor material, column 7 lines 44-45. But Gardner does not expressly disclose a material is from at least one alloy that includes at least two constituents selected from polycrystalline silicon, tungsten, tantalum, copper and gold. At the time of the invention was made; it would have been obvious to one of ordinary skill in the art to use the teaching of Gardner (6,130,454) as claimed, because it would have created functional equivalent gate electrode.

Regarding to claim 10, Gardner discloses a semiconductor device wherein the sidewall dielectric 52 is formed on the side surface section of the gate. But Gardner does not expressly disclose a material including main component, silicon nitride, silicon oxide or a compound thereof. However, Gardner (6,201,278) discloses sidewall 522A and 522B, fig. 5F, is formed from the material including silicon dioxide, column 13 line 28. At the time of the invention was made; it would have been obvious to one of ordinary skill in the art to combine the teaching of Gardner (6,201,278) with Gardner (6,130,454),

because silicon oxide or silicon nitride is being used for dielectric sidewall spacer is well known in the art.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) US Patent 6,355,955 to Gardner et al

b) US Patent 5,869,359 to Prabhakar.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X Le whose telephone number is 703-306-0208. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Thao X. Le
May 22, 2002

PHAT X. CAO
PRIMARY EXAMINER